CT1000
Product Specification

ver.1.0.2

CanTech Inc.

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This draft specification is a function and performance notation concerning capacitive proximity sensor LSI(CT1001). The contents of this draft specification may be subject to change.

Features of this product

This product is a low current consumption LSI using CMOS process.
The internal operation mode can be changed at any time and has high versatility.
It has sleep mode + intermittent operation function, so low power consumption operation is possible.
An output comparator is built in and an interrupt signal is output when the set threshold is exceeded.
A 10-bit AD conversion circuit is built in.
The interface with the CPU is I2C.

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1 Specification

1.1 Absolute Maximum Rating

GND=GNA=0V.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		−0.5		3.9	V
Input voltage	V_{IN}	Terminal applied voltage	−0.5		V_{DD}+0.5	V
Output voltage	V_{OUT}	Terminal applied voltage	−0.5		V_{DD}+0.5	V
Output current	I_O		−20		20	mA
Power consumption	P_C				300	mW
Storage temperature range	T_{STG}	No condensation	−40		125	℃

1.2 Recommended operation conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage range	V_{DD}		2.7		3.6	V
Operating temperature range	T_{OPR}		−20		75	℃

1.3 Electrical characteristics

Unless otherwise noted、V_{DD}=3.3V,GND=GNA=0V,Ta=25℃.

1.3.1 Terminal load specification

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
A electrode load capacitance	C_A	When not detected, vs ground ＊1	2.0		30	pF
B electrode load capacitance	C_B	When not detected, vs ground ＊1	2.0		30	pF
A, B electrode offset capacitance	ΔC_{AB}	When not detected,Ca−Cb	−8		8	pF
Shield electrode load capacitance	C_{SH}	Capacitance vs ground + A, B electrode capacity			250	pF
Output load capacitance	C_{LO}				20	pF
Output load resistance	R_{LO}		10			KΩ

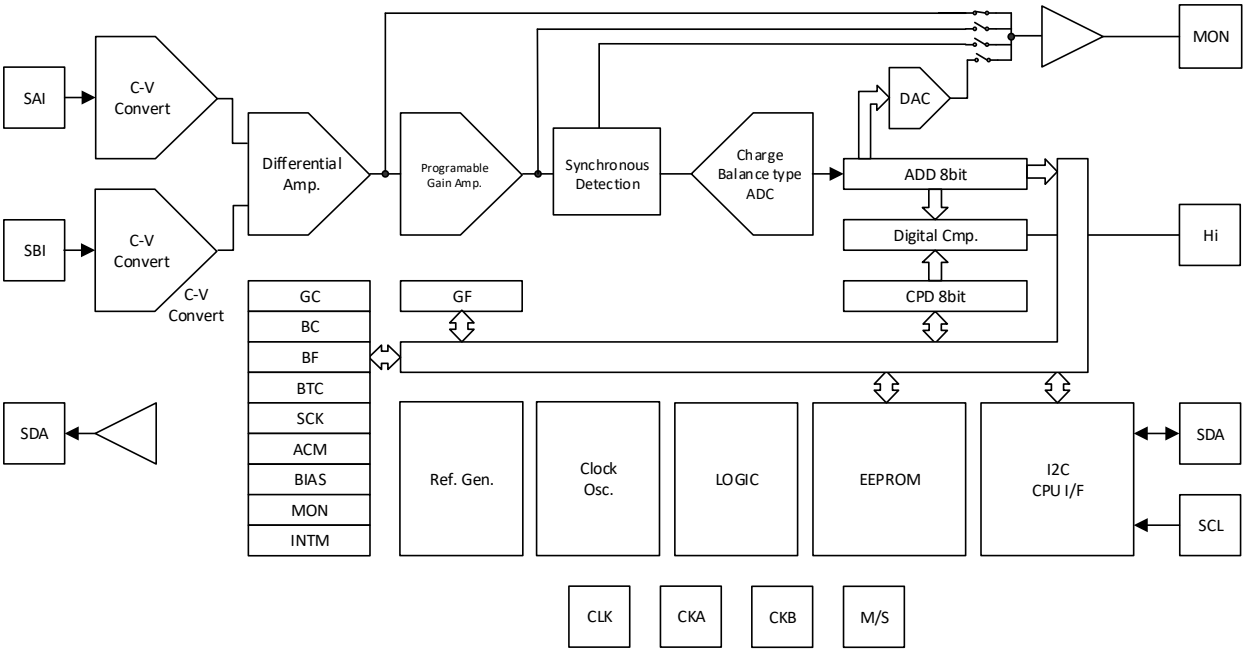
*1 The electrode capacitance that can be connected depends on the setting of "GC".

1.3.2 Conversion characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current consumption (No external load)	I_{DA1}	@f_{CVC}=40KHz ＊2		800	1000	uA
	I_{DA2}	@f_{CVC}=20KHz ＊2		500	800	uA
	I_{SLP}	In sleep mode.			30	uA
C−V conversion frequency	f_{CV1}	「SCK」=1		40		KHz
	f_{CV3}	「SCK」=2		20		KHz
C−V CV conversion capacity	C_{CVC}	2.5,5,10,20pF	2.5		20	pF
Differential amplifier gain	G_{DIF}	2x,4,x8x,16x	2		16	X
Programable amp. gain	G_{PGA}	G_{AD}=1+N/255, N=0～255	1		2	X
Charge transfer capacity	C_{TR}	4,8,16,32pF	4		32	pF
ADC Conversion capacity	C_{ADC}			10		pF
Cumulative count 1	N_{SAM1}	「ACM」=3		8192		回
Cumulative count 2	N_{SAM2}	「ACM」=2		4096		回
Cumulative count 3	N_{SAM3}	「ACM」=1		2048		回
Cumulative count 4	N_{SAM4}	「ACM」=0		1024		回
Overall gain	G_{TT1}		0.001		1	fF/LSB
Sampling time	t_{SMP}	Refer to Table 5-1.				
ADC resolution	R_{ADC}			10		Bit
Temperature coefficient correction range	T_{COEF}		−1000		1000	ppm/℃

＊2: Consumption current depends on the setting of "BIAS".

2 Block Diagram



3 Terminal configuration

No.	Name	I/O	Function
1	GNA	P	Ground
2	CSO	AO	Shield signal output
3	SAI	AI	Electrode A connection terminal
4	SBI	AI	Electrode B connection terminal
5	GNA	P	Analog ground
6	M/S	I	Master / slave setting (L=slave)
7	CKS	I/O	Synchronous clock input/output
8	CLK	I/O	System clock input / output
9	VDD	P	＋Power supply
10	GND	P	Ground
11	SCL	I	I2C synchronous clock input
12	SDA	I/O	I2C Serial data input / output
13	SLP	I	Sleep control (L=Sleep)
14	HI	O	Comparator output
15	MON	AO	Internal voltage monitor output
16	VHF	O	Internal reference voltage monitor

I :Logic input, O :Logic outoput, P :Power supply
AI :Analog input, AO :Analog oiutput

4 Internal register configuration

Address (HEX)	EEPROM Address (HEX)	Name	Function	R/W	No. Of BITs	Remarks
00	00	GC	Coarse gain adjust、+Sign	R/W	8	
01	00	GF	Gain fine adjust	R/W	8	
02	01	BC	Coarse offset adjust	R/W	8	
03	01	BF	Offset fine adjust	R/W	8	
04	02	BTC	Temperature correction	R/W	8	
05	02	MON	Voltage monitor select	R/W	2	
06	03	ADL	ADC result (lower 2 bits)	R	2	
07	03	ADH	ADC result (upper 8 bits)	R	8	
08	04	TF	Temp. sensor offset adjust	R/W	8	
09	04	CM	Output comparate value (MSB 8bit)	R/W	8	
0A	05	SCK	CV Conversion frequency set	R/W	1	
0B	05	ACM	CV Cumulative number	R/W	2	
0C	06	BIAS	Bias current setting	R/W	8	
0D	06	INTM	Intermittent interval	R/W	8	
0E	07					RESERVED
0F	07	I2CADR	I2C Device address register	R/W	7	
10～3F	08～1F					RESERVED
40	–	EPINDX	EEPROM Access Index	R/W	8	
42	–	EPDATAL	EEPROM Access Data L	R/W	8	
43	–	EPDATAH	EEPROM Access Data H	R/W	8	
44	–	EPCTL1	EEPROM Control/Status	R/W	8	
45	–	EPCTL2	EEPROM Control/Status	R/W	8	
46	–	EPCTL3	EEPROM Control/Status	R/W	8	

※ Internal data is 8 bits per address,
In EEPROM, 16 bits of data are stored per address.
Example: In the EEPROM, the BF register value corresponds to the upper 8 bits of the 16 bits of the data of the address 01.

※Writing to the internal register(I2CADR) is performed only by setting the device address in 6.3.2.

4.1 Internal register details

4.1.1 GC: Sensitivity and offset correction polarity setting

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GC	SOFSET	-	Ctr1	Ctr0	Gdif1	Gdif0	Ccvc1	Ccvc0

CV Conversion circuit capacitance value setting. (Sensitivity adjustment)

Ccvc : CV Conversion capacitance

Ccvc1		Ccvc0	Capacitance
L		L	20pF
L		H	10pF
H		L	5pF
H		H	2.5pF

※ Sensor capacitance value that can be connected varies depending on the Ccvc.

20pF : 30pF～8pF
10pF : 15pF～4pF
5pF : 7.5pF～2pF
2.5pF : 3.5pF～1pF

Gdif : Differential amplifier gain

Gdif1	Gdif0	magnification
L	L	2
L	H	4
H	L	8
H	H	16

Ctr:Charge transfer capacity

Ctr1	Ctr0	Capacitor
L	L	4pF
L	H	8pF
H	L	16pF
H	H	32pF

SOFSET:Polarity switching of offset correction. The correction direction in BC, BTC registers changes.
L:SBI>SAI H:SAI>SBI

4.1.2 GF

ADC conversion gain adjustment function. Correction is possible within 1 to 2 times range.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GF	GF7	GF6	GF5	GF4	GF3	GF2	GF1	GF0

G_{AD}=1+(GF)/255 GF:DEC(0～255)

4.1.3 BC

Coarse offset adjustment function. Up to 8 pF can be corrected with 8 bits.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BC	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Input correction capacitance value =8×(BC)/255 [pF] BC:DEC (0～255)

4.1.4 BF

Offset fine adjustment function. 40 fF can be corrected with 8 bits.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BF	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

Input correction capacitance value = 40 × (BF) / 255 [fF] BC: DEC (0 to 255)

4.1.5 BTC

Correct offset fluctuation with temperature in the range of ± 1000 ppm / ° C maximum.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BTC	BTC7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0

Input corrected capacitance temperature coefficient =−1000+2000(BTC)/255 [PPM/℃] BC:DEC (0～255)

4.1.6 MON

The internal voltage to be monitored can be selected with the MON pin.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MON	−	−	−	−	−	−	MON1	NON0

MON1	MON0	MON output
L	L	Analog output voltage
L	H	Differential stage output
H	L	Internal reference potential
H	H	Temperature sensor output

4.1.7 ADL,ADH

ADC Store register. ADL:Lower 2bit、ADH:Upper 8BIT(Read only)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADL	AD1	AD0	−	−	−	−	−	−

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

4.1.8 TF

Correct the offset of the temperature sensor output.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TF	TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0

Temperature sensor output:VTS=VDD/2+(T−25)*0.005+(−0.5+(TF)/255) [V]
T:温度 TF: DEC (0～255)

4.1.9 CM

Comparison value storage register
When the ADH register value exceeds the value set by the CM register value, the HI terminal output becomes Hi.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CM	CM7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0

"HI"Terminal Hi@ADH＞CM、 Lo@ADH≦CM

4.1.10 SCK

Set the C−V conversion frequency.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCK	−	−	−	−	−	−		SCK0

SCK0	CVConversion frequency
L	40KHz
H	20KHz

4.1.11 ACM

You can set the cumulative number of CV conversion results.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACM	–	–	–	–	–	–	ACM1	ACM0

ACM1	ACM0	Cumulative count
L	L	1024
L	H	2048
H	L	4096
H	H	8192

4.1.12 BIAS

Set the bias current.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS	BIAS7	BIAS6	BIAS5	BIAS4	BIAS3	BIAS2	BIAS1	BIAS0

By adjusting the bias current according to the CV conversion period it is possible to operate with excessive or insufficient current consumption.

Internal bias current value =Imax-Imax×(BIAS)/255 BIAS:DEC (0～255)

※Since the internal bias current hardly flows near the register value 255, the circuit operation becomes unstable. Please adjust while checking circuit operation.

4.1.13 INTM

Set the intermittent operation mode.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS	BIAS7	BIAS6	BIAS5	BIAS4	BIAS3	BIAS2	BIAS1	BIAS0

During intermittent operation, it enters a sleep state, resulting in low current consumption.

Intermittent time＝tcv×(INTM) tcv:Conversion time. INTM:DEC(0～255)

※INTM＝0:It becomes continuous operation.

4.1.14 EPINDEX、EPDATAL、EPDATAH、EPCTL1～3

This is EEPROM access register.

Details are described in Chapter 8 EEPROM Specification.

5 Function details

5.1 AD value conversion gain

10-bit AD conversion output. The capacitance value per 1 LSB is
(CCVC * CADC)/ (GDIF * CTR * GAD * 12.22) / 1024 [pF/LSB]

With minimum sensitivity CCVC=40pF,CADC=10pF,GDIF=2,CTR=4pF,GAD=1
(40*10)/(2*4*1*12.22)/1024=0.004pF/LSB

With maximum sensitivity CCVC=5pF,CADC=10pF,GDIF=16,CTR=32pF,GAD=2
(5*10)/(16*32*2*12.22)/1024=0.0039fF/LSB

5.2 CV conversion frequency and conversion time

The cumulative frequency of CV conversion frequency and CV conversion result is set by the register of "SCK" and "ACM" shown in the previous section. The conversion time of one cycle changes depending on the contents of these two registers.

Table 5-1, Cumulative frequency and conversion time

CV Conversion frequency	Cumulative number			
	8192	4096	2048	1024
40KHz	205msec	102msec	51msec	25msec
20KHz	410msec	205msec	102msec	51msec

5.3 Control of current consumption

When the CV conversion frequency is set high, high speed operation is required for the internal circuit. Conversely, setting the CV conversion frequency low does not require high-speed operation.
High-speed operation requires more current consumption. Current consumption can be adjusted by adjusting the operating speed with "BIAS" register.
It is possible to select the necessary and sufficient current consumption according to the CV conversion frequency.

5.4 Internal Voltage Monitor

Outputs analog output voltage, differential output, internal reference potential, built-in temperature sensor output voltage to "MON" terminal by switching "MON" register.

MON	00	01	10	11
Select output	Output voltage	Differential stage output	Internal reference	Temperature sensor

5.5 Intermittent operation

If a value other than "0" is set in the "INTM" register, intermittent operation is performed.
During intermittent operation, it enters a measurement stop state, resulting in low current consumption.
The intermittent time is "N" times (N = 1 to 255) of the conversion time shown in Table 5-1.
After the intermittent time has elapsed, the conversion operation is performed once, and the operation that goes to the Measurement stop state again is repeated.
The Measurement stop state state starts immediately after the operation is completed and ends after one sampling period before the next operation start.

5.6 Synchronous clock

When using two or more of this product, it may interfere with each other if the detection electrodes are installed close to each other.
In such a case, please use it in the synchronous mode. The synchronous mode is controlled by the "M / S" terminal. Connect the "M / S" terminal other than one of the multiple devices (master) to GND. In addition, connect "CLK" and "CKS" of all the elements to each other.

A synchronous clock is output from "CLK" "CKS" of the master element and input to other elements. As a result, all elements operate synchronously.

6 SLEEP

General features

When "SLP" terminal is set to "Low", all functions except the built-in register stop. In this state, current consumption is only the data retention of the built-in register, which is extremely slight.
If you return the "SLP" terminal from low to high, all functions will work again. The recovery time is maximum 20 msec.

7 EEPROM Specification

Register configuration

The EEPROM is mounted inside this LSI and has the function of transferring data stored in the EEPROM to the internal function register immediately after turning on the power supply.

Access to the on-chip EEPROM is a register indirect method, and access is performed using three types of index register, data register, and control register.

7.1 Register configuration

Table 7.1 shows the register list of this LSI.

ADDR is the address of the register, R = Read Only W = Write Only R / W Read, Write.

Table 7.1 EEPROM controle register

ADDR	R/W	Symbol	EEPROM ADDR	Name	b7	b6	b5	b4	b3	b2	b1	b0
40 h	R/W	EPINDX	–	EEPROM Access Index	A7	A6	A5	A4	A3	A2	A1	A0
42 h	R/W	EPDATAL	–	EEPROM Access Data L	D7	D6	D5	D4	D3	D2	D1	D0
43 h	R/W	EPDATAH	–	EEPROM Access Data H	D15	D14	D13	D12	D11	D10	D9	D8
44 h	R/W	EPCTL1	–	EEPROM Control/Status	STS	EPBER	EPER	EPBW	EPARW	EPWR	EPARR	EPRD
45 h	R/W	EPCTL2	–	EEPROM Control/Status	EPENSTS	EPCPON	–	–	–	–	EPDS	EPEN
46 h	R/W	EPCTL3	–	EEPROM Control/Status	EETEST	VEE2	VEE1	–	–	–	–	EPCTL

7.1.1 Register Details

7.1.1.1 EEPROM Access Index Register [EPINDX]

Function	EEPROM store index for access								
Address	40 h								
Description	Specify EEPROM address								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	A7	A6	A5	A4	A3	A2	A1	A0
	bit Name	Description							
	A[7:0]	EEPROM address							
	Initial	00 h							

7.1.1.2 EEPROM Access Data Register [EPDATAL]

Function	Data storage for EEPROM								
Address	42 h								
Description	For storing data to be written or read data								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	D7	D6	D5	D4	D3	D2	D1	D0
	bit Name	Descriptions							
	D[7:0]	Write Write data to EEPROM Read Read data from EEPROM							
	Initial	00 h							

7.1.1.3 EEPROM Access Data Register [EPDATAH]

機 能	Data storage for EEPROM access								
アドレス	43 h								
説 明	For storing data to be written or read data								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	D15	D14	D13	D12	D11	D10	D9	D8
	bit Name	DEscription							
	D[7:0]	Write Write data to EEPROM Read Read data from EEPROM							
	Initial	00 h							

7.1.1.4 EEPROM Control/Status Register [EPCTL1]

Function	Operation designation / status information acquisition of EEPROM								
Address	44 h								
Description	Reads the operating state of the EEPROM, and controls operations such as batch register transfer When 1 is written to the control bit simultaneously, the operation is executed with the following priority order.EPRD→EPARR→EPWR→EPARW→EPBW→EPER→EPBER								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	STS	EPBER	EPER	EPBW	EPARW	EPWR	EPARR	EPRD
	– :retains the written contents								
	bit Name	Description							
	STS	Operating state of EEPROM							
		=0	In idling						
		=1	Working						
	EPBER	Block erasing in progress							
	EPER	Address erase specified by register “EPINDX”							
	EPBW	Writes the contents of the EPDATA register to the EEPROM at the block address specified by the EPINDX register ※1							
	EPARW	Writes the contents of the register to EEPROM all at once							
	EPWR	Writes the contents of the EPDATA register to the EEPROM at the address specified by the EPINDX register							
	EPARR	Collectively store from EEPROM to read register							
	EPRD	Data is read from the EEPROM address specified by the EPINDX register and stored in the EPDATA register							
	Initial	00 h							

When controlling the EEPROM, write 1 to the EPEN bit of the EPCTL 2 register and put it in controllable state.
After completing the EEPROM control, write 1 to the EPDS bit of the EPCTL 2 register and put it in the standby state.

※1

Each time the EPCTL bit in the EPCTL 3 register is turned ON / OFF, the register address is incremented by 2 addresses.
To write all registers, the EPCTL bit must be turned ON / OFF twice the number of registers ÷ 2 times.

7.1.1.5 EEPROM Control/Status Register [EPCTL2]

Function	Operation specification of EEPROM								
Address	45 h								
Description	Perform control during programming and erasing of EEPROM								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R	R	–	–	–	–	W	R/W
	bit Name	EPENSTS	EPCPSTS	–	–	–	–	EPDS	EPEN
	– : Written contents are retained								
	bit Name	Description							
	EPENSTS	Controllable in EEPROM control state 1							
	EPDS	Set to EEPROM control disabled state							
	EPEN	By setting 1 to the EEPROM controllable state, it becomes possible state.							
	Initial	00 h							

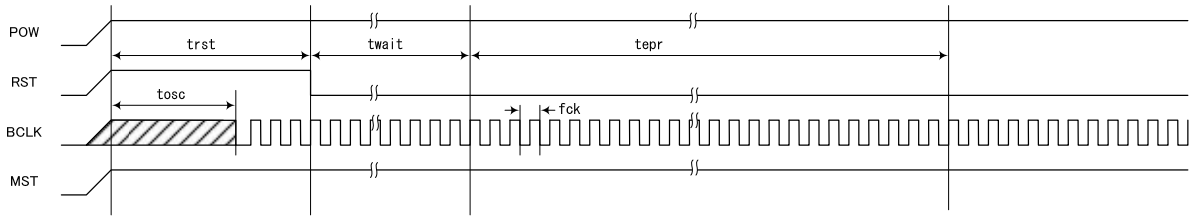
7.1.1.6 EEPROM Control/Status Register [EPCTL3]

Function	Operation specification of EEPROM								
Address	46 h								
Description	Perform control during programming and erasing of EEPROM								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	–	–	–	–	R/W
	bit Name	EETEST	VEE2	VEE1	–	–	–	–	EPCTL
	– : Written contents are retained								
	bit Name	Description							
	EETEST	For test Be sure to write 0 to this bit							
	VEE2								
	VEE1								
	EPCTL	Time system for writing and erasing御 When the write operation or the erase operation is specified by the EPCTL1 register, operation is started by setting this bit to 1, and 0 is written to this bit to end the operation. Set this bit to 1 during Min. 4 mS, Max. 8 mS.							
	Initial	00 h							

7.2 Operation explanation

7.2.1 Power-on action

After turning on the power supply, data is transferred from the EEPROM to the internal register at once, after the reset of the internal circuit is released.



Item	Symbol	time			unit	Remarks
		min	typ.	max		
Oscillation stabilization time	tosc			TBD	uS	
Oscillation period	fck		320	1000	KHz	
Reset release time	trst	150		400	uS	Since VDD exceeds 90%
Time from reset release until EEPROM read start	twait		10		Cycle	
Read time from EEPROM	tepr		512		Cycle	

7.2.2 Common subject

Before accessing the EEPROM, set the [EPCTL 2] register, EPEN bit to 1, and put the EEPROM in controllable state.

When access to the EEPROM is completed, set the [EPCTL 2] register and EPDS bit to 1 and put the EEPROM in the standby state.

7.2.3 Control inhibit / enable operation

To access the EEPROM, set the EPEN bit in the [EPCTL 2] register to 1.

After completion of the control, set the EPDS bit of [EPCTL 2] register to 1.

7.2.4 Read

To read directly from the EEPROM, the EEPROM contents are transferred to the data register by setting the address to be read in the [EPINDX] register and writing 1 to the EPRD bit of [EPCTL 1].

During transfer from the EEPROM to the data register, the EPRD bit in the control register is held at 1 and cleared to 0 after the transfer is completed.

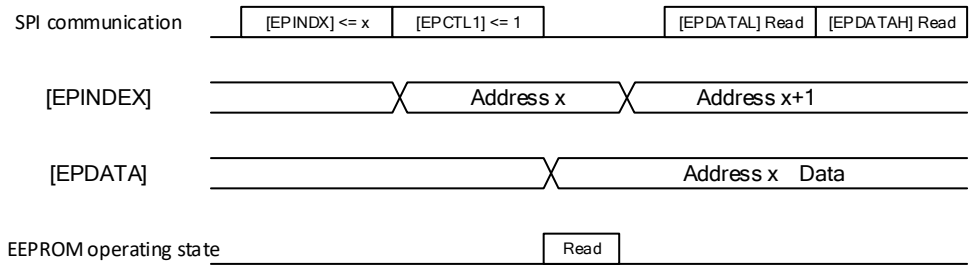


Fig. 8.1 Read sequence

7.2.5 Write

In order to write data directly to the EEPROM, set the address of the EEPROM to write to the [EPINEX] register and the data to write to the [EPDATA] register, respectively, set the EPWR bit of the [EPCTL 1] register to 1 and set the [EPCTL 3] register By turning EPCTL bit ON → OFF, data is written to EEPROM.

Turn on the EPCTL bit during Min. 4 mS, Max. 8 mS.

If it is less than the above time, it may not be written.

If it exceeds the above time, the rewriting life of the EEPROM will be shortened.

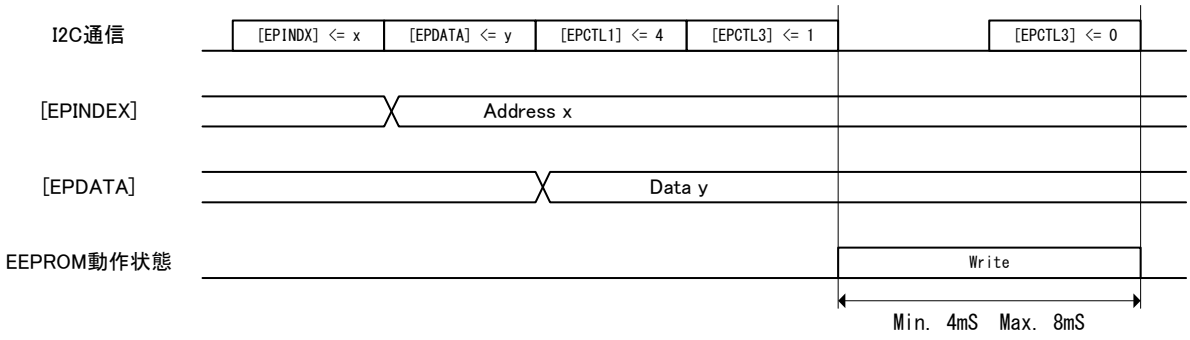


Fig. 8.2 Write sequence

7.2.6 Erase

Erase specific address of EEPROM.

Set the address of the EEPROM to be erased in the [IPINDX] register, erase it by setting the EPWR bit of the [EPCTL 1] register to 1 and turning the EPCTL bit of the [EPCTL 3] register ON → OFF.

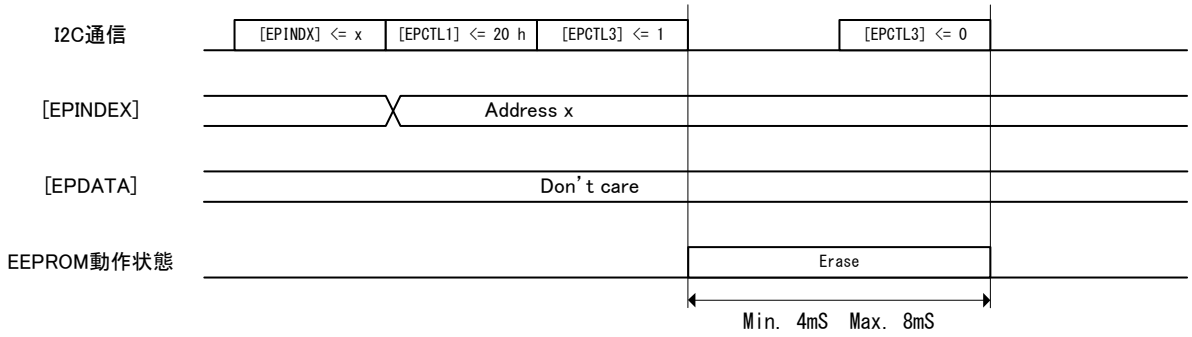


Fig. 8 Erase sequence

7.2.7 Batch write

The contents of the internal registers are collectively written to the EEPROM. Undefined data is written to the address where the register does not exist. Writing 1 to the EPARW bit of the [EPCTL 1] register and repeating ON / OFF of the EPCTL bit of the [EPCTL 3] register writes the contents of the register to the EEPROM in units of 2 bytes.

By transferring 64 bytes, batch writing is completed.

To terminate halfway, write 0 to the [EPCTL1] register and clear it.

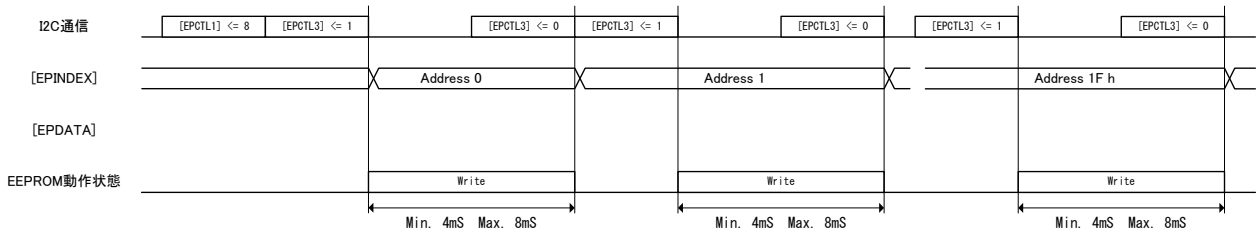


Fig. 8.4 *Batch write* sequence

7.2.8 Block erase

Batch erase of EEPROM is performed.
Write 1 to the EPBER bit of the [EPCTL 1] register and turn ON / OFF the EPCTL bit of the [EPCTL 3] register.

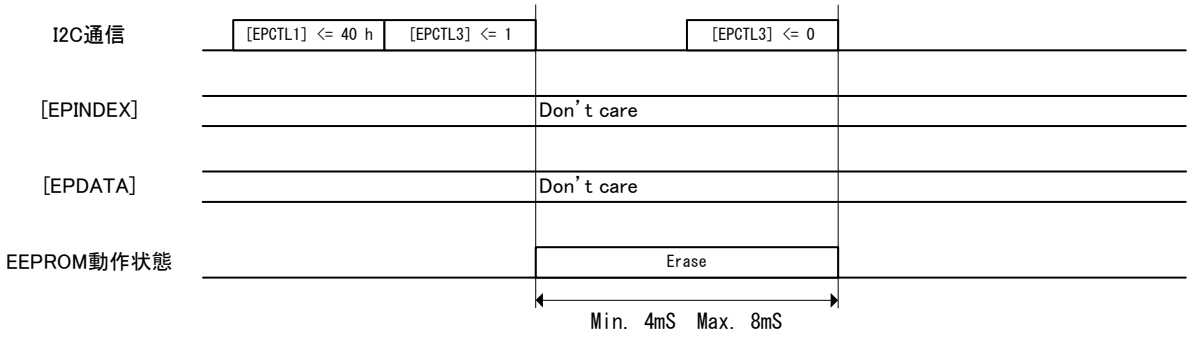


Fig. 8.5 *Block erase* sequence

7.2.9 Block write

Writes the contents of the [EPDATA] register to all addresses of the EEPROM.
Write 1 to the EPBWR bit of the [EPCTL1] register and turn ON / OFF the EPCTL bit of the [EPCTL 3] register.

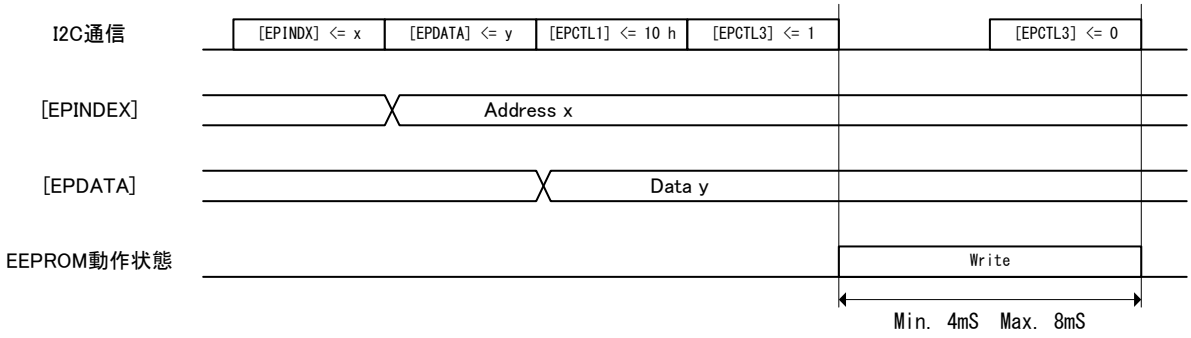


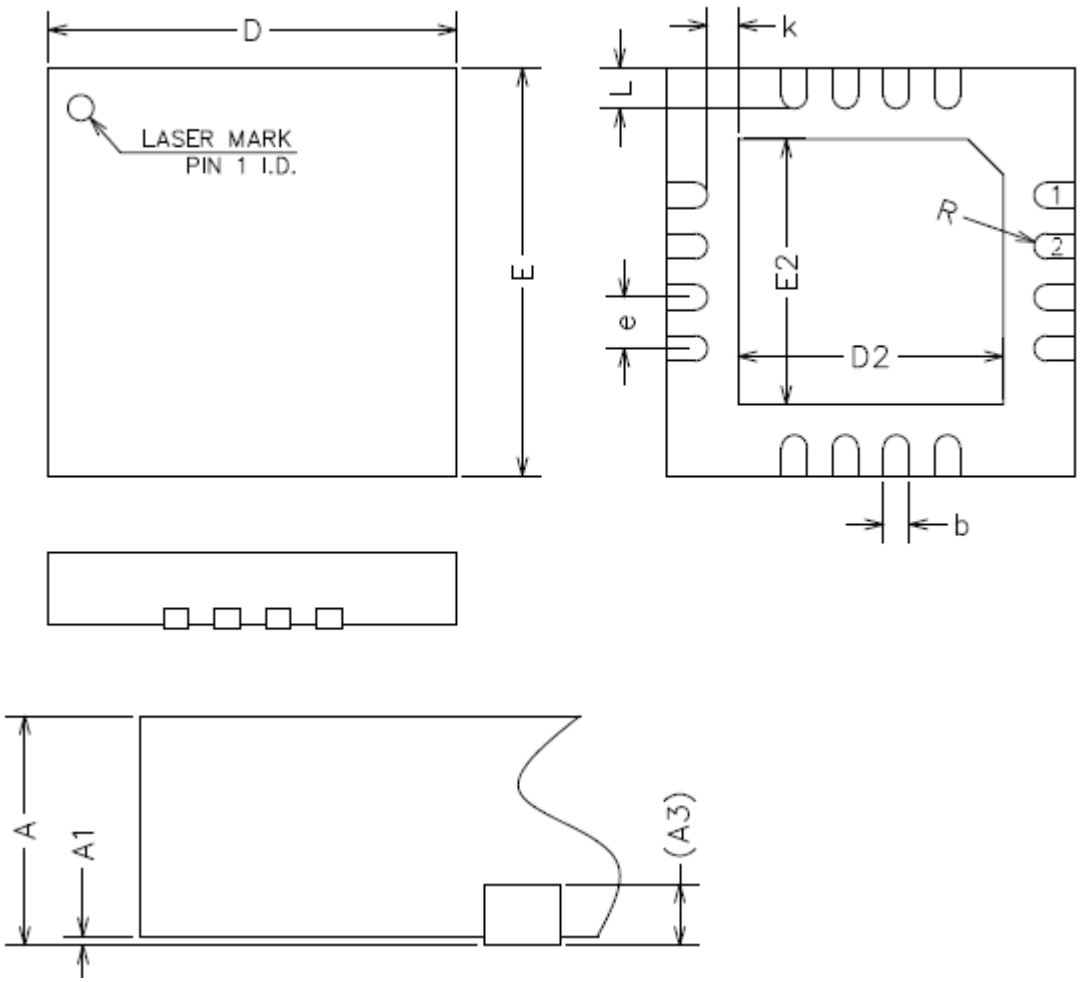
Fig. 8.6 Block write sequence

7.3 Characteristics

Item	min.	max.	Unit
Write / erase time	4	8	ms
Data retention period	10		Year
No. of write / erase@25℃	$1x10^5$		
No. of write / erase@125℃	$1x10^4$		
Operating temperature range	-40	125	℃

8 External dimensions

WQFN16 Package



(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–