AT1089

Product specification

ver.1.1

CanTech Inc.

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This specification is a function and performance notation for AT1089 capacitive proximity sensor LSI. The contents of this specification are subject to change.

Features

This product is a low current consumption LSI using CMOS process.
The internal operation mode can be changed at any time and it has high versatility.
As a capacitive proximity sensor, outstanding detection distance can be realized.
It has an intermittent operation function and low power consumption operation is possible.
An output comparator is built in and an interrupt signal is output when the set threshold is exceeded.
10-bit AD conversion circuit is built in.
The interface with the CPU adopted I2C.

1. Specification

Absolute Maximum Ratings GND=GNA=0V.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		-0.5		3.9	V
Input voltage	V_{IN}	Terminal applied voltage	-0.5		V_{DD}+0.5	V
Output votage	V_{OUT}	Terminal applied voltage	-0.5		V_{DD}+0.5	V
Output current	I_O		-20		20	mA
Power consumption	P_C				300	mW
Storage temperature	T_{STG}	No condensation	-40		125	℃

Recommended conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.7		3.6	V
Operating temperature	T_{OPR}		-20		75	℃

Electrical characteristics

Otherwise noted : V_{DD}=VDA=3.3V,GND=GNA=0V,Ta=25℃.

1.1 Terminal load specification

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
A electrode capacity	C_A	not detected, capacity to ground *1	2.0		60	pF
B electrode capacity	C_B	not detected, capacity to ground *1	2.0		60	pF
A, B electrode offset capacity	ΔC_{AB}	When not detected, Ca－Cb	-8		8	pF
S electrode capacity	C_{SH}	Ground capacitance + A, B electrode			250	pF
Output load capacity	C_{LO}				20	pF
Output load resistance	R_{LO}		10			KΩ

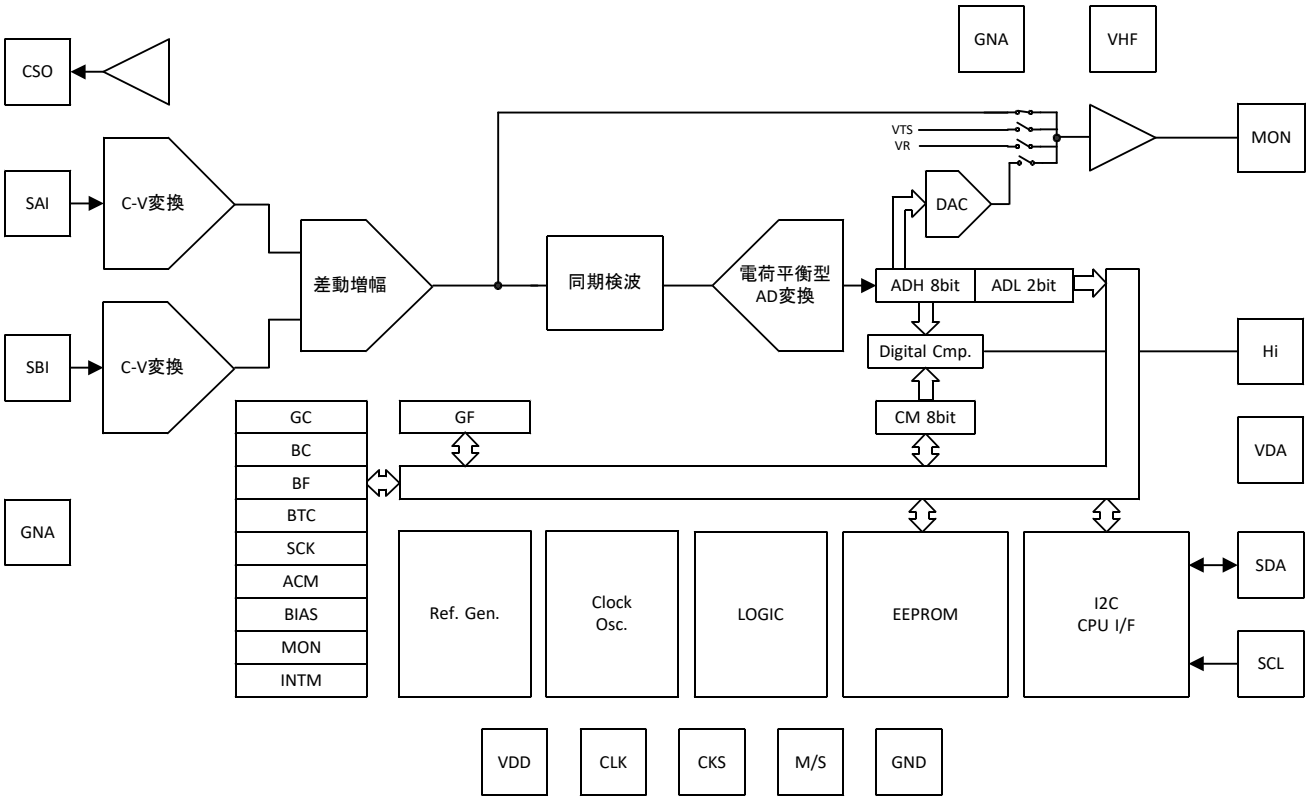
*1 The electrode capacity that can be connected depends on the setting contents of "GC" (lower 2 bits).

1.2 Conversion characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Consumption current 1	I_{DA1}	No external load,f_{CVC}=160KHz＊2		1200	2000	uA
Consumption current 2	I_{DA2}	No external load, f_{CVC}=20KHz＊2		500	800	uA
Consumption current 3	I_{DA3}	0n sleep		100		uA
CV conversion frequency 1	f_{CV1}	[SCK]=0		160		KHz
CV conversion frequency 2	f_{CV2}	[SCK]=1		80		KHz
CV conversion frequency 3	f_{CV3}	[SCK]=2		40		KHz
CV conversion frequency 4	f_{CV4}	[SCK]=3		20		KHz
CV conversion capacity	C_{CVC}	5,10,20,40pF	5		40	pF
Difference amplifier gain	G_{DIF}	2x,4,x8x,16x	2		16	dB
AD conversion gain	G_{PGA}	G_{AD}=1+N/255, N=0～255	0		6	dB
Charge transfer capacity	C_{TR}	4,8,16,32pF	4		32	pF
CB type ADC integral capacity	C_{ADC}			10		pF
Cumulative number 1	N_{SAM1}	[ACM]=3		8192		
Cumulative number 2	N_{SAM2}	[ACM]=2		4096		
Cumulative number 3	N_{SAM3}	[ACM]=1		2048		
Cumulative number 4	N_{SAM4}	[ACM]=0		1024		
Total gain	G_{TT1}		0.004		3.9	fF/LSB
Sampling time	t_{SMP}	Refer to “Table 5-1”				
AD conversion resolution	R_{ADC}			10		Bit
Temperature correction range	T_{COEF}		-1000		1000	ppm/℃

＊2: Current consumption depends on the setting of "BIAS".

2. Block Diagram



3. Terminal configuration

No.	Name	I/O	Functional overview
1	NC	−	Open (No connect)
2	GNA	P	Ground terminal
3	CSO	AO	Shield voltage output
4	SAI	AI	Proximity sensor A electrode connection terminal
5	SBI	AI	Proximity sensor B electrode connection terminal
6	GNA	P	Analog ground
7	M/S	I	Master / slave setting (L = slave)
8	CKS	I/O	Synchronous clock input / output
9	CLK	I/O	System clock input / output
1 0	NC	−	Open (No connect)
1 1	NC	−	Open (No connect)
1 2	VDD	P	+ Power supply terminal
1 3	GND	P	Ground terminal
1 4	SCL	I	I2Cbus synchronous clock signal input
1 5	SDA	I/O	I2CbusSerial data input / output
1 6	VDA	O	+ Analog power supply terminal
1 7	HI	O	Comparative output
1 8	MON	AO	Internal voltage monitor output
1 9	VHF	O	Internal reference voltage moniter
2 0	NC	−	Open (No connect)

I:Logic input terminal, O:Logic output terminal P:Power supply terminal
AI:Analog input terminal, AO:Analog output terminal

4. Internal register configuration

Internal register list

Address (HEX)	EEPROM Address (HEX)	Name	Function	R/W	Effective bits	Remarks
00	00	GC	CV conversion gain rough adjustment,& Offset polarity	R/W	8	
01	00	GF	Gain fine adjustment	R/W	8	
02	01	BC	Offset coarse adjustment	R/W	8	
03	01	BF	Offset fine adjustment	R/W	8	
04	02	BTC	Temperature correction factor setting	R/W	8	
05	02	MON	Internal voltage monitor selection	R/W	2	
06	03	ADL	AD conversion result (lower 2 bits)	R	2	Move to MSB
07	03	ADH	AD conversion result (upper 8 bits)	R	8	
08	04	TF	Temperature sensor offset adjustment	R/W	8	
09	04	CM	Output comparison value (upper 8 bits)	R/W	8	
0A	05	SCK	CV conversion frequency settingCV conversion result cumulative number	R/W	2	
0B	05	ACM	CV conversion result cumulative number	R/W	2	
0C	06	BIAS	Bias current setting	R/W	8	
0D	06	INTM	Intermittent operation interval	R/W	8	
0E	07					RESERVED
0F	07	I2CADR	I2C device address storage register	R/W	7	
10～3F	08～1F					RESERVED
40	-	EPINDX	EEPROM Access Index	R/W	8	
42	-	EPDATAL	EEPROM Access Data L	R/W	8	
43	-	EPDATAH	EEPROM Access Data H	R/W	8	
44	-	EPCTL1	EEPROM Control/Status	R/W	8	
45	-	EPCTL2	EEPROM Control/Status	R/W	8	
46	-	EPCTL3	EEPROM Control/Status	R/W	8	

※ Internal data is 8 bits per address,
In EEPROM, 16 bits of data are stored per address.
Example: In the EEPROM, the BF register value corresponds to the upper 8 bits of the 16 bits of the data of the address 01.

＊ Writing to the I2CADR register is performed only by setting the device address in 6.3.2.

4.1. Internal register details

4.1.1. G C

Sensitivity setting and offset correction polarity setting

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GC	SOFSET	-	Ctr1	Ctr0	Gdif1	Gdif0	Ccvc1	Ccvc0

Capacitance value setting of CV conversion circuit. (Sensitivity adjustment)

Ccvc：CV conversion capacity

Ccvc 1	Ccvc 0	Capacitance value
L	L	40pF
L	H	20pF
H	L	10pF
H	H	5pF

※ CcvcSensor capacitance value that can be connected varies depending on the capacitance value.
40pF：60pF～16pF
20pF：30pF～8pF
10pF：15pF～4pF
5pF ：7.5pF～2pF

Gdif：Difference amplifier gain

Gdif1	Gdif0	magnification
L	L	2
L	H	4
H	L	8
H	H	16

Ctr：Charge transfer capacity

Ctr1	Ctr0	Capacitance value
L	L	4pF
L	H	8pF
H	L	16pF
H	H	32pF

SOFSET：Polarity switching of offset correction.
BC、BF、BTC The correction direction in the register changes.
L:SBI>SAI H:SAI>SBI

4.1.2. G F

AD conversion gain adjustment function It can be corrected in the range of 1 to 2 times.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GF	GF7	GF6	GF5	GF4	GF3	GF2	GF1	GF0

G_{AD}=1+(GF)/255 [x] GF:DEC(0～255)

4.1.3. B C

Coarse offset adjustment function. Up to 8 pF can be corrected with 8 bits.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BC	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Input correction capacitance value=8×(BC)/255 [pF] BC:DEC (0～255)

4.1.4. B F

Offset fine adjustment function　40 fF can be corrected with 8 bits.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BF	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

Input correction capacitance value=40×(BF)/255　[fF]　BC:DEC (0～255)

4.1.5. B T C

Correct offset fluctuation with temperature in the range of ± 1000 ppm/℃ maximum.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BTC	BTC7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0

Input correction capacitance temperature coefficient=-1000+2000(BTC)/255　[PPM/℃]　BC:DEC (0～255).

4.1.6. M O N

The internal voltage to be monitored with the MON pin can be selected.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MON	-	-	-	-	-	-	MON1	NON0

MON 1	MON 0	MON output
L	L	Analog output voltage
L	H	Differential stage output
H	L	Internal reference voltage
H	H	Temperature sensor output

4.1.7. A D L、A D H

ADC output value storage register ADL:Lower 2 bits,ADH:The upper 8 BIT is stored.(Read only)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADL	AD1	AD0	-	-	-	-	-	-

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

4.1.8. T F

Correct the offset of the temperature sensor output.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TF	TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0

Temperature sensor output VTS=VDD/2+（T-25）*0.005+(-0.5+(TF)/255) [V]
T:temperature　TF: DEC (0～255)

4.1.9. C M

When the ADH register value exceeds the value set by the CM register value, the HI terminal output becomes Hi.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CM	CM7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0

HITerminal=Hi ＠ADH＞CM、　HITerminal=Lo ＠ADH≦CM

4.1.10. S C K

You can set the CV conversion frequency.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCK	-	-	-	-	-	-	SCK1	SCK0

SCK1	SCK0	CVConversion frequency
L	L	160KHz
L	H	80KHz
H	L	40KHz
H	H	20KHz

4.1.11. A C M

You can set the cumulative number of CV conversion results.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACM	-	-	-	-	-	-	ACM1	ACM0

ACM 1	ACM 0	Cumulative count
L	L	1024
L	H	2048
H	L	4096
H	H	8192

※ The output value is smoothed as the cumulative count is increased,
Conversion time per cycle becomes longer.

4.1.12. B I A S

Set bias current of internal circuit.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS	BIAS7	BIAS6	BIAS5	BIAS4	BIAS3	BIAS2	BIAS1	BIAS0

By adjusting the bias current according to the CV conversion period, it is possible to operate with excessive or insufficient current consumption.

Internal bias current value=Imax-Imax×(BIAS)/255　BIAS:DEC (0～255)

* Since the internal bias current does not flow near the register value 255, the circuit operation becomes unstable.

4.1.13. I N T M

Sets the intermittent operation mode.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BIAS	BIAS7	BIAS6	BIAS5	BIAS4	BIAS3	BIAS2	BIAS1	BIAS0

During intermittent operation, it enters a sleep state, resulting in low current consumption.

Intermittent time=tcv×(INTM)　tcv：Conversion time of one cycle　INTM：DEC（0～255）

※INTM＝It becomes continuous operation at 0.

4.1.14.EPINDEX、EPDATAL、EPDATAH、EPCTL1～3

This register is for accessing EEPROM.

Details are described in Chapter 8 EEPROM Specification.

5. Detail of function

5.1. AD conversion gain

The capacitance value per 1 LSB of AD conversion output of 10 bits is as follows
（CCVC * CADC）/ (GDIF * CTR * GAD * 12.22) / 1024 [pF/LSB]

With minimum sensitivity, CCVC=40pF,CADC=10pF,GDIF=2,CTR=4pF,GAD=1
(40*10)/(2*4*1*12.22)/1024=0.004pF/LSB

With maximum sensitivity,　CCVC=5pF,CADC=10pF,GDIF=16,CTR=32pF,GAD=2
(5*10)/(16*32*2*12.22)/1024=0.0039fF/LSB

5.2. CV conversion frequency and conversion time

The cumulative frequency of CV conversion frequency and CV conversion result is set by the register of "SCK" and "ACM" shown in the previous section. The conversion time of one cycle varies depending on the contents of these two registers.

Table 5-1, Cumulative frequency and conversion time

CVConversion frequency	Cumulative number			
	8192	4096	2048	1024
160KHz	51msec	25msec	12.5msec	6.3msec
80KHz	102msec	51msec	25msec	12.5msec
40KHz	205msec	102msec	51msec	25msec
20KHz	410msec	205msec	102msec	51msec

5.3. Control of current consumption

When the CV conversion frequency is set high, high speed operation is required for the internal circuit. Conversely, setting the CV conversion frequency low does not require high-speed operation.
High-speed operation requires more current consumption. Current consumption can be adjusted by adjusting the operating speed with "BIAS" register.
It is possible to select the necessary and sufficient current consumption according to the CV conversion frequency.

5.4. Internal voltage monitor

Outputs analog output voltage, differential output, internal reference potential, built-in temperature sensor output voltage to "MON" terminal by switching "MON" register.

MON	00	01	10	11
Output	Output voltage	Differential stage output	Internal reference potential	Temperature sensor output

5.5. Intermittent operation

If a value other than "0" is set in the "INTM" register, intermittent operation is performed.
During intermittent operation, it enters a sleep state, resulting in low current consumption.
The intermittent time is "N" times (N = 1 to 255) of the conversion time shown in Table 5-1.
After the intermittent time has elapsed, the conversion operation is performed once, and the operation that goes to the sleep state again is repeated.

5.6. The sleep state starts immediately after the operation is completed and ends after one sampling period before the next operation start.

5.7. Synchronous clock

When two or more products are used at the same time, if the detection electrodes are placed close together, they may interfere with each other.

In such a case, please use in the synchronous mode. The synchronous mode is controlled by the "M / S" terminal. Connect the "M / S" terminal other than one of the multiple devices (master) to GND. In addition, connect "CLK" and "CKS" of all the elements to each other.

A synchronous clocks are output from "CLK" "CKS" of the master element and input to other elements. This ensures that all elements operate synchronously.

6. About the I2C bus

6.1.1.1 General features

Both SDA and SCL are bidirectional lines and are connected to the positive supply voltage via parallel resistors.

When the bus is open both lines are in the "H" state.

The output stage of the device connected to the bus requires an open drain to execute the AND connection function.

In the I2C bus, it is possible to transfer data of 100 kbit / s in standard mode, up to 400 kbit / s in fast mode and 3.4 Mbit / s in high speed mode.

This LSI supports first mode.

The number of interfaces connected to the bus is limited only by the bus's maximum capacitance (400 pF).

6.1.1.2 Bit transfer

Devices using different processes (CMOS, NMONS, bipolar, etc.) can be connected to the I 2 C bus, so if the logic value "0" ("L") and "1" ("H") levels are constant It is determined by the level of VDD.

One clock pulse is generated for each data bit transferred.

6.1.1.3 Data validity

While the clock is "H", the state of the SDA line must be constant. The state of the data line changes between "H" and "L" only when the clock signal on the SCL line is "L". (refer to the figure below)

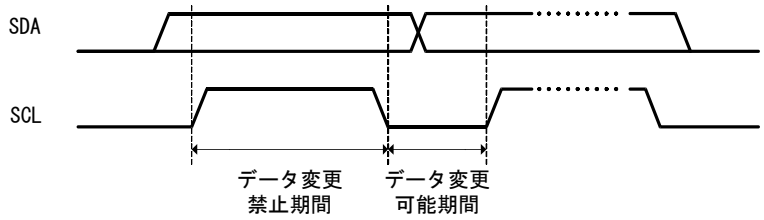


Figure 6-1

6.1.1.4 『"START" condition and "STOP" condition

"START" condition

It shows a state where the SDA line changes from "H" to "L" when SCL is "H"

"STOP" condition

Indicates a state where the SDA line changes from "L" to "H" when SCL is "H"

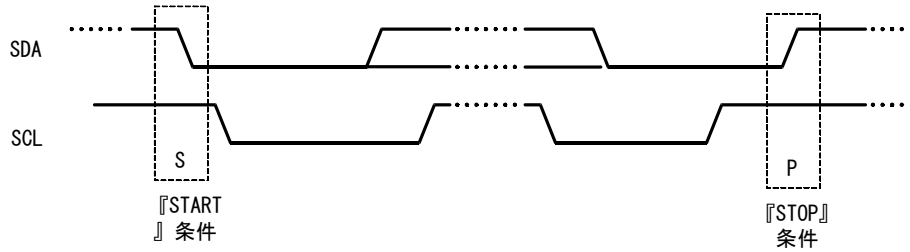


Figure 6-2

Each condition is always generated by the master.
After the "START" condition occurs, the bus goes into a busy state and the bus is released after the "STOP" condition is generated.
Besides this, "repeat" START "condition" exists.

The repetitive "START" condition means that the I2C bus normally allows generation of a state equivalent to the "START" condition at the timing when the "STOP" condition occurs.
If the "repeat" START "condition" is generated, the bus will not be released.

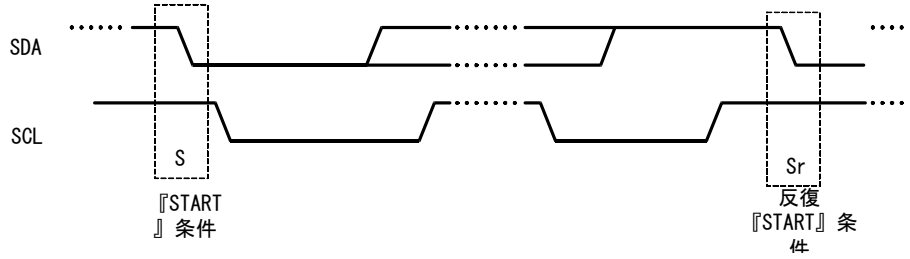


Figure 6-3

6.1.1.5 Byte format

The length of each frame outputted on the SDA line is always 9 bits, and it consists of a data byte (8 bits) and a response bit. There is no limit on the number of frames that can be transmitted in one transfer, and any number of bytes can be transmitted.
An acknowledge bit is required after each byte.
Data is transmitted in order from the most significant bit (MSB).
The receiver can keep the clock line SCL "L" and place the transmitter in the wait state.

6.1.1.6 Acknowledge

An acknowledgment is always required when transferring data. Clock pulses for acknowledgment are generated by the master. When an acknowledge clock pulse is generated, the transmitter opens the SDA line.
The receiver must set the SDA line to "L" so that the SDA line is stable in the "L" state when the acknowledge clock pulse is in the "H" state.

An addressed receiver MUST generate an acknowledge every time each byte ends, unless the message starts with a CBUS address.
If the slave / receiver can not confirm the address, the data line SDL must be kept "H" (= released).
At this time, the master can generate a "STOP" condition to generate an iteration "START" condition to abort the transfer of data or to start a new transfer.

When the slave / receiver confirms the address and can not receive the data byte during the transfer, it notifies the master by not generating the acknowledgment.
When the master becomes a receiver, it notifies the slave of the end of data by not acknowledging the last data byte transmitted from the slave.
At this time, the slave must release the SDL line.

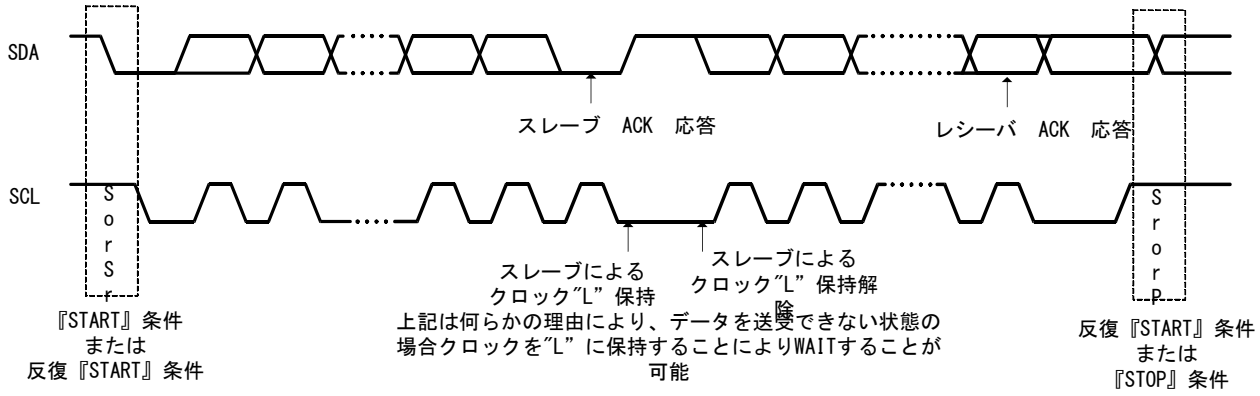


Figure 6-3

6.1.1.7 Bit address format

For data transmission, the address of the slave is transmitted after the "START" condition. This address is composed of seven bits, and the eighth bit is followed by a data direction bit (R / W). (Let 8 bits be the first byte)

When R / W = '0', it becomes data reception (slave / receiver) from the master, and when R / W = '1', it becomes data transmission (slave · transmitter) to the master.

First byte

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
Slave address							direction

The first reserved byte has the following reserved address

Slave address							R/W bit	Description
b6	b5	b4	b3	b2	b1	b0		
0	0	0	0	0	0	0	0	General call address
0	0	0	0	0	0	0	1	Start byte
0	0	0	0	0	0	1	x	CSUB address
0	0	0	0	0	1	0	x	Reserved for different bus formats
0	0	0	0	0	1	1	x	Reserved for future use
0	0	0	0	1	x	x	x	Hs mode master code
1	1	1	1	1	x	x	x	Reserved for future use
1	1	1	1	0	x	x	x	10ビットスレーブアドレス指定

Table 6-1

Notes

This LSI prohibits setting of all the above addresses.
Operation is not guaranteed if it is set.
However, the general call address is used to set the device address.

6.1.1.8 Timing

Refer to later chapter, I2C electrical characteristic

6.2 II2C bus transmission procedure

This LSI performs various processing according to the command transmitted from the master based on the I2C specification.

The transmission procedure will be described below.

6.2.1.Receiver · transmitter common operation

Receiver · transmitter common operation

However, reading status is valid

The processing that takes time for the main internal operation is described below.

・ • EEPROM access operation (during power supply rise sequence)

6.2.2.Receiver operation

It receives the first byte (device address) from the master and compares it with the address of this LSI. In case of coincidence, the L / W bit is judged (= '0'), this LSI becomes a receiver and returns ACK (= '0') and waits for the next byte reception. (In the receiver operation, the byte following the first byte is always the register address specification byte.)

Next, it takes in the data byte, writes ACK (= '0') to the specified address received earlier, and increments the internal address.

Subsequent data bytes are sequentially written to the incremented address.

Receive format

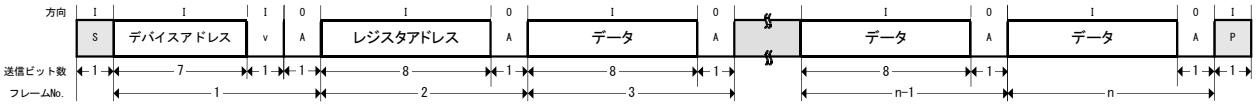


Figure 6-4

Explanation of symbols

S: "START" condition or repeat "START" condition

R / W: Data direction specification bit (= '0')

A: Acknowledge (ACK)

N: No acknowledge (NACK)

P: "STOP" condition, repeated "START" condition

I: Reception

O: Send

In principle, n of transmit / receive bits is 8 bits, but in mixed connection with CBUS, 1 ≦ n in CBUS specification.

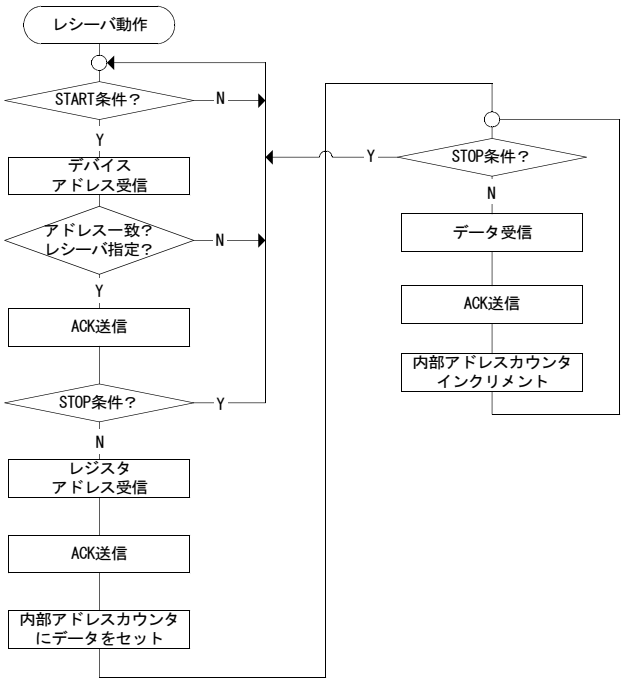
Since this LSI does not support CBUS compatibility, CBUS addressing is prohibited. If a CBUS compatible address is received, it will not respond.

If the number of received frames is 2, set the register address pointer to prepare for the next transmitter designation request.

When the number of received frames is 2 or more, the specified register address is incremented every ACK reply, and the received data is written.

There is an ACK response even if the register does not exist at the specified address.

It returns to 00 H when the specified address exceeds the upper limit (FF H).


レシーバ動作
START条件？
N
Y
デバイス
アドレス受信
アドレス一致？
レシーバ指定？
N
Y
ACK送信
STOP条件？
Y
N
レジスタ
アドレス受信
ACK送信
内部アドレスカウンタ
にデータをセット
STOP条件？
Y
N
データ受信
ACK送信
内部アドレスカウンタ
インクリメント

6.2.3. Transmitter operation

Receives the first byte from the master and compares it with the specified address of this LSI.
In case of coincidence, the L / W bit is judged (= '1'), the LSI becomes a transmitter, returns ACK (= '0'), and transmits data by the succeeding clock.
At this time, the data to be transmitted transmits the contents of the register address received by the receiver operation.
After reset, if no receiver operation is specified, transmit data at address 0.
After the ACK reply, the master sends NACK and then transmits until "STOP" condition or repeated "START" condition occurs.
The data to be transmitted is based on the designation of the specified register address. When an address without register exists, the validity of the data is not guaranteed. (It becomes indefinite data)
If the response from the master is "ACK", prepare the following data, and in the case of "NACK", transmission ends.

Transmission format

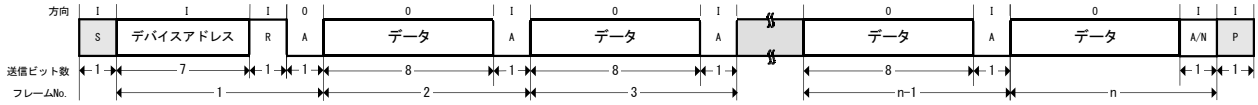


Figure 6-5

Explanation of symbols

S: "START" condition or repeat "START" condition
SLA: Slave address
R / W: Data direction specification bit (= '1')
A: Acknowledge (ACK)
N: No acknowledge (NACK)
P: "STOP" condition, repeated "START" condition
I: Reception
O: Send

Transmission bit n is 8 bits

Since this LSI does not support CBUS compatibility, CBUS addressing is prohibited. If a CBUS compatible address is received, it will not respond.

The number of transfer frames is 1 or more and no upper limit is specified in the I2C standard.

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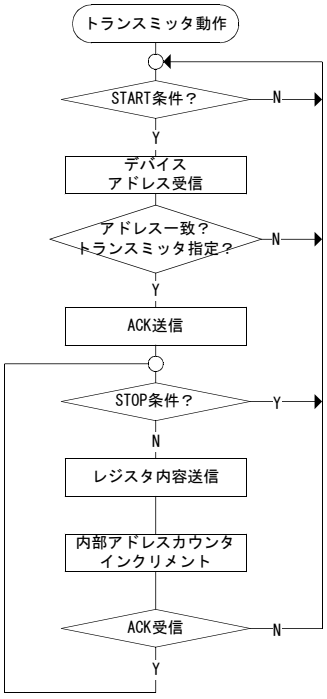
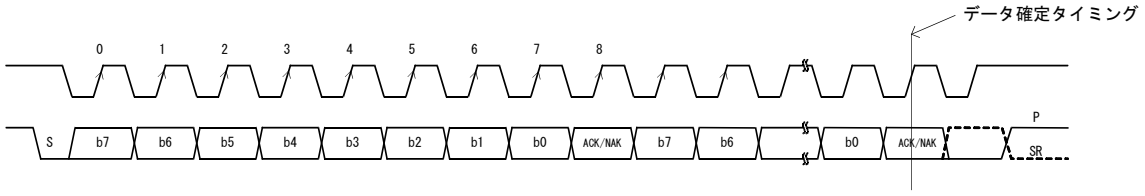


6.3. Internal operation

6.3.1. Register set timing

The operation start timing for each interface is shown below.

I2C I/F

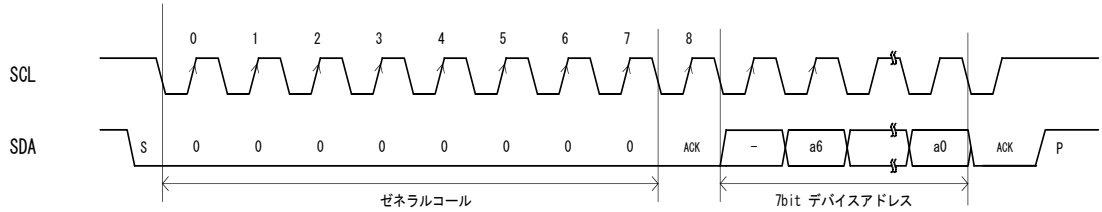


Operation starts within 3 system clocks from the above data determination timing

6.3.2. Device address setting

When the first byte (general call address) is received from the master, the next second byte is recognized as the device address of this LSI and transferred to the device address register.

Note) The master does not transmit after the second byte. (It ends with STOP condition)



Device address setting timing

※ Be sure to set the device address at initial setting.
Setting the device address data in the EEPROM (I 2 CAD register) makes it unnecessary to set the next time or later.
When changing the device address, re-enter another correction register value.

7. I2C bus electrical characteristics

7.1. I2C bus AC characteristics

I2C I / F specification is posted below (From Phillips' material)

AC characteristics

Item	Symbol	High speed mode		Unit
		MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeat) "START" condition Generate the first clock pulse after this period	$t_{HD;STA}$	0.6	-	μs
SCL During the "L" period of the clock	t_{LOW}	1.3	-	μs
SCL During the "H" period of the clock	t_{HIGH}	0.6	-	μs
Setup time for repetitive "START" condition	$t_{SU;DAT}$	0.6	-	μs
Data setup time	t_{BUF}	100(1)	-	ns
SDA & SCL Signal rise time	f_r		300	ns
SDA & SCL Fall time of signal	t_f		300	ns
Setup time of "STOP" condition	$t_{SU;STO}$	0.6	-	ns
Bus free time between "START" condition and "START" condition	t_{BUF}	1.3	-	μs
The pulse width of the spike suppressed by the input filter	t_{SP}	0	50	ns

Table 7-1

(1) (1) Fast mode I 2 C bus devices can be used for standard mode I 2 C bus system, but the required condition tSU; DAT ≧ 250 ns must be satisfied. This means that the device automatically does not extend the "L" period of the SCL signal. When a certain device does not extend the "L" period of the SCL signal, tr (max) + tSU; DAT = 1000 + 250 = 1250 ns (according to the I 2 C bus specifications in the standard mode data bits) than when the SCL line is released Previously, the following data must be output on the SDA line.

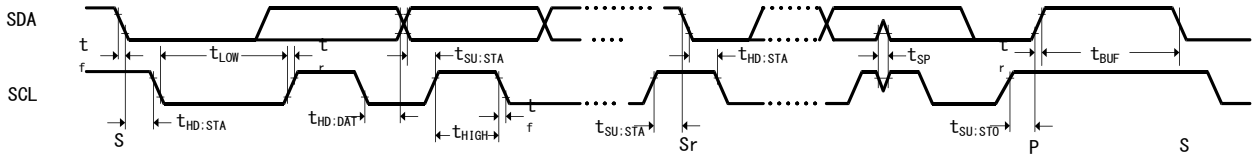


Figure 7-1

8. EEPROM specification

Overview

The EEPROM is mounted inside this LSI and has the function of transferring data stored in the EEPROM to the internal function register immediately after power is turned on.

Access to the on-chip EEPROM is a register indirect method, and access is performed using three types of index register, data register, and control register.

8.1. Register configuration

Table 8-1 shows the register list of this LSI.

ADDR is the address of the register, R = Read Only, W = Write Only, R / W Read, Write

Table 8-1 EEPROM Control register list

ADDR	R/W	Symbol	EEPROM ADDR	名 称	b7	b6	b5	b4	b3	b2	b1	b0
40 h	R/W	EPINDX	-	EEPROM Access Index	A7	A6	A5	A4	A3	A2	A1	A0
42 h	R/W	EPDATAL	-	EEPROM Access Data L	D7	D6	D5	D4	D3	D2	D1	D0
43 h	R/W	EPDATAH	-	EEPROM Access Data H	D15	D14	D13	D12	D11	D10	D9	D8
44 h	R/W	EPCTL1	-	EEPROM Control/Status	STS	EPBER	EPER	EPBW	EPARW	EPWR	EPARR	EPRD
45 h	R/W	EPCTL2	-	EEPROM Control/Status	EPENSTS	EPCPON	-	-	-	-	EPDS	EPEN
46 h	R/W	EPCTL3	-	EEPROM Control/Status	EETEST	VEE2	VEE1	-	-	-	-	EPCTL

8.1.1. Register Details

8.1.1 EEPROM Access Index Register [EPINDX]

Function	EEPROM Store index for access								
Address	40 h								
Description	Specify the EEPROM address for accessing the EEPROM								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	A7	A6	A5	A4	A3	A2	A1	A0
	bit Name	**Description**							
	A[7:0]	EEPROM read / write address							
	Initial value	00 h							

8.1.2 EEPROM Access Data Register [EPDATAL]

Function	EEPROM Storage of access data								
Address	42 h								
Description	Specify data to be written to EEPROM and read data for EEPROM read								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	D7	D6	D5	D4	D3	D2	D1	D0
	bit Name	**Description**							
	D[7:0]	When writing Write data to EEPROM When reading Read data from EEPROM							
	Initial value	00 h							

8.1.3 EEPROM Access Data Register [EPDATAH]

Function	EEPROM Storage of access data								
Address	43 h								
Description	Specify data to be written to EEPROM and read data for EEPROM read								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	D15	D14	D13	D12	D11	D10	D9	D8
	bit Name	**Description**							
	D[7:0]	When writing Write data to EEPROM When reading Read data from EEPROM							
	Initial value	00 h							

6.1.4 EEPROM Control/Status Register **[EPCTL1]**

Function	Operation designation / status information acquisition of EEPROM								
Address	44 h								
Description	Reads the operating state of the EEPROM, and controls operations such as batch register transfer When 1 is written to the control bit at the same time, the operation is executed with the following priority order. EPRD→EPARR→EPWR→EPARW→EPBW→EPER→EPBER								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	bit Name	STS	EPBER	EPER	EPBW	EPARW	EPWR	EPARR	EPRD
	- retains the written contents								
	bit Name	**Description**							
	STS	Operating state of EEPROM (or output of b 6 to b 0 -)							
		=0	**Idling in progress**						
		=1	in action						
	EPBER	Block address erase							
	EPER	Address erase specified by EPINDX register							
	EPBW	Writes the contents of EPDATA register to EEPROM at the block address specified by EPINDX register * 1							
	EPARW	Write the contents of register at once to EEPROM							
	EPWR	Writes the contents of the EPDATA register to the EEPROM at the address specified by the EPINDX register							
	EPARR	Collectively store from EEPROM to read register							
	EPRD	Data is read from the EEPROM address specified by the EPINDX register and stored in the EPDATA register							
	Initial value	00 h							

When controlling the EEPROM, write 1 to the EPEN bit of the EPCTL 2 register and put it in controllable state. After completing the EEPROM control, write 1 to the EPDS bit of the EPCTL 2 register and put it in the standby state.

※1

Each time the EPCTL bit in the EPCTL 3 register is turned ON / OFF, the register address is incremented by 2 addresses.ます。

To write all registers, the EPCTL bit must be turned ON / OFF twice the number of registers ÷ 2 times.

8.1.5 EEPROM Control/Status Register **[EPCTL2]**

Function	Operation specification of EEPROM								
Address	45 h								
Description	Perform control during programming and erasing of EEPROM								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R	R	-	-	-	-	W	R/W
	bit Name	EPENSTS	EPCPSTS	-	-	-	-	EPDS	EPEN
	- retains the written contents								
	bit Name	**Description**							
	EPENSTS	Controllable in EEPROM control state 1							
	EPDS	Set to EEPROM uncontrollable state							
	EPEN	By setting 1 to EEPROM controllable state, it becomes possible state.							
	Initial value	00 h							

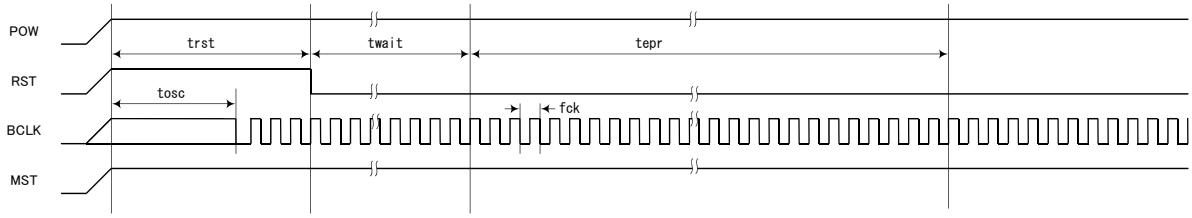
8.1.6 EEPROM Control/Status Register **[EPCTL3]**

Function	Operation specification of EEPROM								
Address	46 h								
Description	Perform control during programming and erasing of EEPROM								
Bit field	bit No.	b7	b6	b5	b4	b3	b2	b1	b0
	R/W	R/W	R/W	R/W	-	-	-	-	R/W
	bit Name	EETEST	VEE2	VEE1	-	-	-	-	EPCTL
	- retains the written contents								
	bit Name	**Description**							
	EETEST	For TEST Be sure to write 0 to this bit							
	VEE2								
	VEE1								
	EPCTL	Time control during writing and erasing When writing or erasing operation is specified by the EPCTL1 register, operation is started by setting this bit to 1, and 0 is written to this bit to end the operation. Set this bit to 1 during Min. 4 mS, Max. 8 mS.							
	Initial value	00 h							

8.2. Operation explanation

8.2.1. Power on operation

After turning on the power supply, data is transferred from the EEPROM to the internal register at once, after the reset of the internal circuit is released.



Item	Sym bol	Time			Unit	Remarks
		min	typ.	max		
Oscillation stabilization time	tosc			TBD	uS	
Oscillation period	fck		320	1000	KHz	
Reset release time	trst	150		400	uS	
Time from reset release until EEPROM read start	twait		10		Cycle	
Read time from EEPROM	tepr		512		Cycle	

8.3 Common subject matter

Before accessing the EEPROM, set the [EPCTL 2] register and EPEN bit to 1, and put the EEPROM in controllable state.

When access to the EEPROM is completed, set the [EPCTL 2] register and EPDS bit to 1 and put the EEPROM in the standby state.

8.4 Control inhibit / enable operation

To access the EEPROM, set the EPEN bit in the [EPCTL 2] register to 1.

After completion of the control, 1 is set to the EPDS bit of the [EPCTL 2] register.

8.5 Read operation

In order to read directly from the EEPROM, the contents of the EEPROM are transferred to the data register by setting the address to be read in the [EPINDX] register and writing 1 to the EPRD bit of [EPCTL 1].

During the transfer from EEPROM to the data register, the EPRD bit of the control register is held at 1 and cleared to 0 after the transfer is completed.

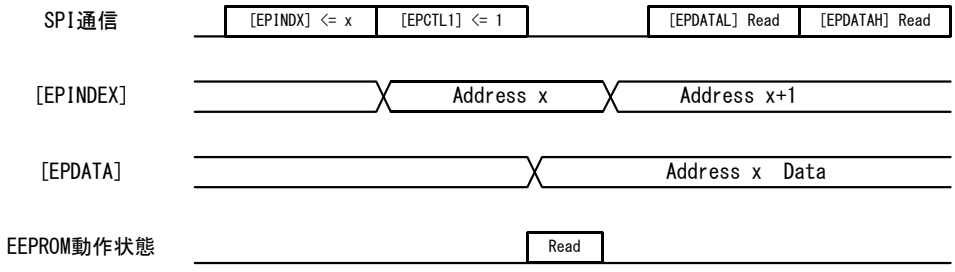


Figure 8-1 Read sequence

8.6 Write operation

To write data directly to the EEPROM, set the address of the EEPROM to write to the [EPINEX] register and the data to write to the [EPDATA] register, respectively, set the EPWR bit of the [EPCTL 1] register to 1 and set the [EPCTL 3] register By turning EPCTL bit ON → OFF, data is written to EEPROM.
Turn on the EPCTL bit during Min. 4 mS, Max. 8 mS.
If it is less than the above time, it may not be written.
If it is longer than the above time, the rewriting life of the EEPROM will be shortened.

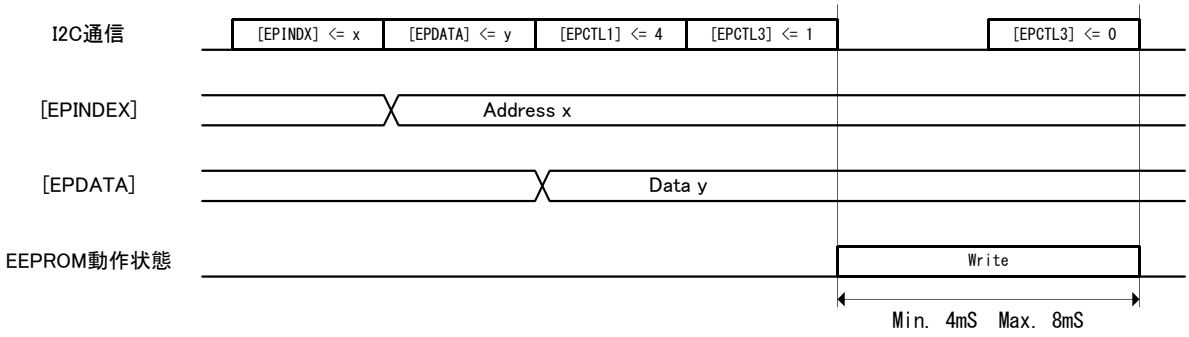


Figure 8-2 Write sequence

8.7 Erase operation

Erases specific address of EEPROM.
It is erased by setting the address of the EEPROM to be erased in the [IPINDX] register, setting 1 to the EPWR bit of the [EPCTL 1] register and turning the EPCTL bit of the [EPCTL 3] register ON → OFF.

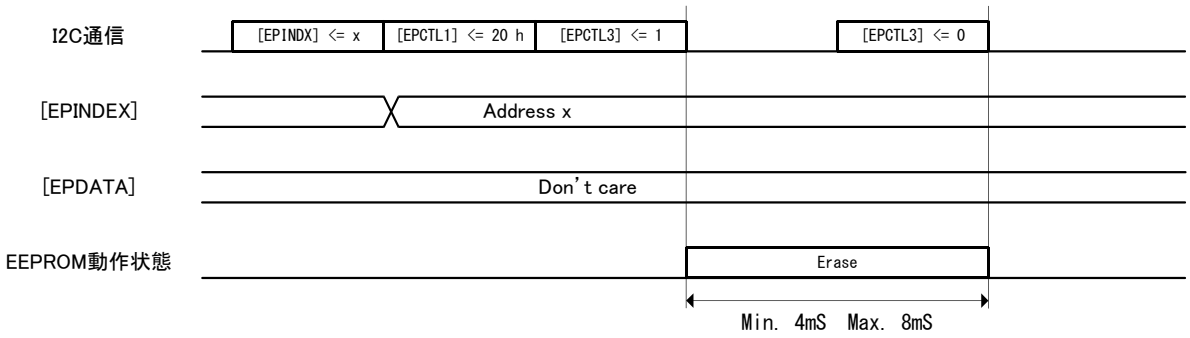


Figure 8-3 Erase operation

8.8 Batch write operation

The contents of the internal registers are collectively written to the EEPROM.
Undefined data is written to addresses that do not have registers.
Writing 1 to the EPARW bit of the [EPCTL 1] register and repeating ON / OFF of the EPCTL bit of the [EPCTL 3] register writes the contents of the register to the EEPROM in units of 2 bytes.
By transferring 64 bytes, batch writing is completed.
To terminate halfway, write 0 to the [EPCTL1] register and clear it.

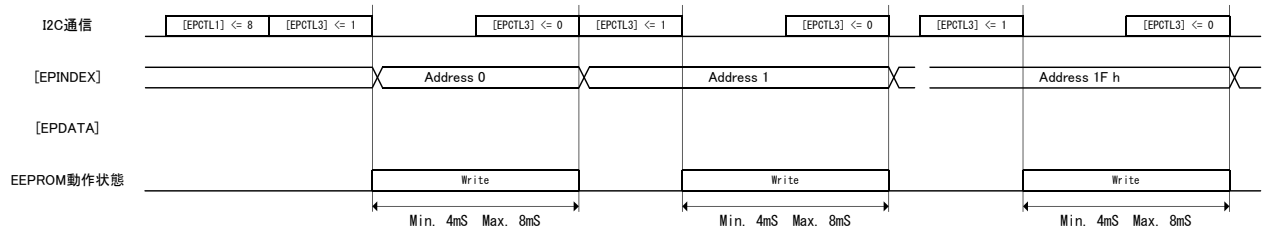


Figure 8-4 Block write operation

8.9 Block write sequence

Batch erase of EEPROM is performed.

Write 1 to the EPBER bit of the [EPCTL 1] register and turn ON / OFF the EPCTL bit of the [EPCTL 3] register.

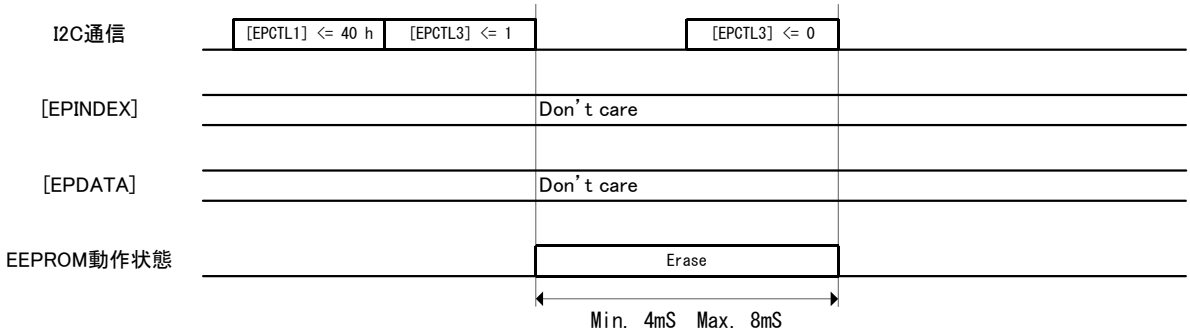


Figure 8-5 Block erase operation

8.10 Block write

[EPDATA] Writes the contents of register to all addresses of EEPROM.

Write 1 to the EPBWR bit of the [EPCTL1] register and turn ON / OFF the EPCTL bit of the [EPCTL 3] register.

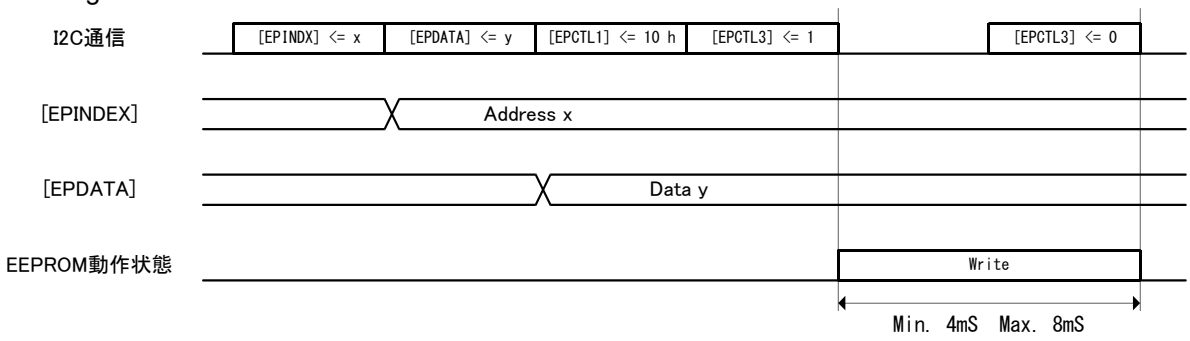


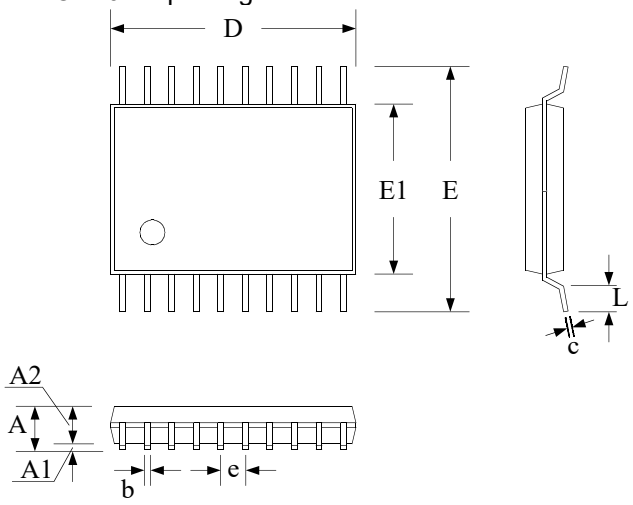
Figure 8-6 Block write operation

8.11. Characteristic

Item	min.	max.	Unit
Write / erase time	4	8	ms
Data retention period	10		year
Number of write / erase@25℃	$1x10^5$		
Number of write / erase@125℃	$1x10^4$		
Temperature range	-40	125	℃

9. External dimensions

TSSOP20Pin package



	min.	typ.	max.
D	6.4		6.6
E	6.2		6.6
E1	4.3		4.5
A			1.2
A1	0.05		0.15
A2	0.95	1	1.05
L	0.45	0.6	0.75
b	0.16	0.22	0.31
e		0.65	
c	0.09		0.2